

WAFER SCALE EXFOLIATION OF MONOCRYSTALLINE MICRO-SCALE SILICON FILMS

Martin J. Ward¹ and Michael A. Cullinan¹

¹Department of Mechanical Engineering

The University of Texas at Austin

Austin, Texas, United States of America

INTRODUCTION

This paper presents the development and simulation of a wafer scale exfoliation process and tool. The method uses an electroplated nickel tensile layer to propagate a crack across a wafer and produce exceptionally cost-effective single-crystal silicon thin films. The system produces silicon films with a thickness of between 5 μm and 35 μm across a 4 inch wafer.

The development of single crystal silicon thin-films creates opportunities for a variety of applications that take advantage of the resulting combination of flexibility and high performance. The process described here is particularly cost-effective compared to other methods of creating thin-film Si, such as etching or mechanical grinding, which further increases the envelope of applications, including flexible solar cells and wearable electronics [1,2]. Silicon exfoliation involves peeling the top layer off a wafer, including any device built into the surface. This approach has the advantage of leveraging existing semi-conductor fabrication techniques to produce flexible devices while other flexible device manufacturing methods require the development of completely new manufacturing procedures.

The exfoliation process is represented in Figure 1. In this process, an adhesion layer of titanium

and a seed layer of nickel are evaporated onto a wafer and on top of any already fabricated devices. Then an approximately 30 μm layer of nickel is electroplated on top of the wafer. Electroplating is a cost-effective process, but it results in some thickness variation. Most of this variation is then removed by laser cutting the outer perimeter off; resulting in an approximately 3 inch wafer. The wafer is then heat treated to induce a residual tensile stress in the nickel. The process is designed such that this stress is just below the required amount to cause spontaneous exfoliation of the silicon wafer. After heat treating a specific external load is applied to exfoliate the film in a controlled manner in order to maintain uniformity and regulate thickness. A new tool is being designed to precisely apply this load.

PROTOTYPE TOOL DESIGN

Previous versions of this process used a wedge or blade-like tool to apply extra stress near the crack front [3]. This produced friction and vibrations that introduced roughness into the exfoliated surface. Other groups used a tape handle layer to apply a peeling force by hand [4]. When tested, this produced inconsistency in the load and exfoliation results, but reduced roughness. Therefore, to overcome these limitations, a tool that could replicate controlled peeling-like loads was proposed.

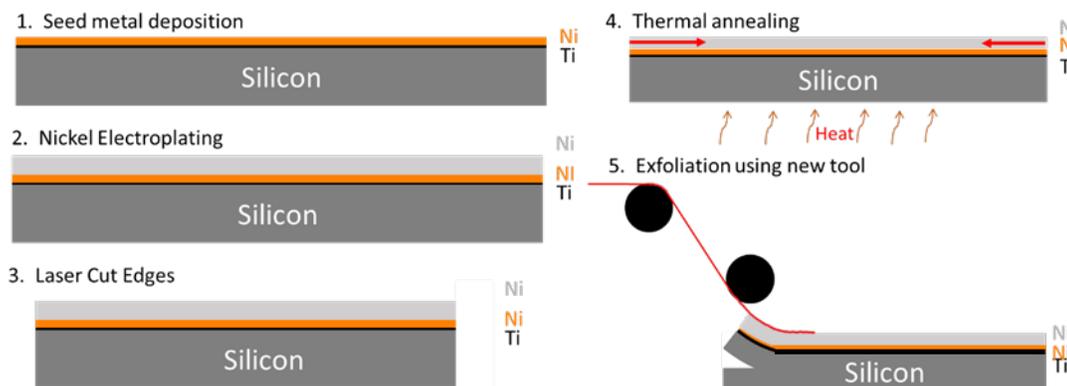


FIGURE 1. Exfoliation process flow

Design

To test this idea a prototype tool was built (shown in Figure 2) that could maintain a constant exfoliation angle, force, and speed. The tool was designed to be quickly manufactured and widely configurable to rapidly test different exfoliation concepts so that in the future a more advanced tool can be designed around the best one. The tool features a simple, adjustable roller design attached to a linear actuator. The roller heights and resulting angle are measured and clamped manually. The exfoliation force is set by clamping the handle film at a set preload, but a system for actively measuring the load during exfoliation is in the process of being added.

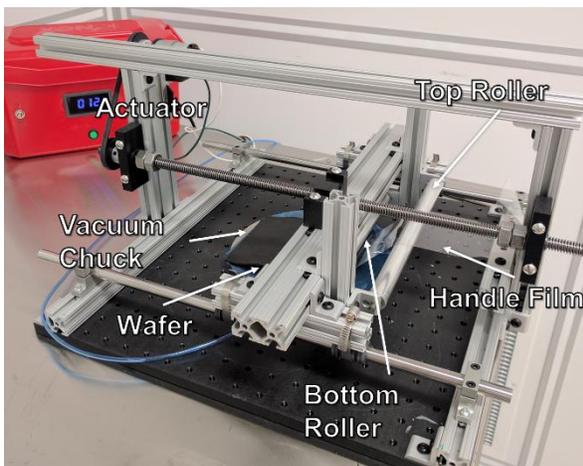


FIGURE 2. New exfoliation tool prototype

The wafer is flattened and adhered to a glass slide with double-sided adhesive polyimide tape and then secured with a vacuum chuck. The glass and tape are necessary because atmospheric air pressure is not enough to flatten the wafer that has been bowed by the tensile stress in the nickel. The flatten state creates a repeatable fixturing and helps define the stresses in the system. A handle film is then attached to the nickel surface with adhesive tape and the two-roller design moves the film across the wafer while maintaining a constant peeling angle and force to propagate the crack front. See Figure 1 for a side view of the roller configuration. Exfoliation speed can be adjusted via the PWM controller of the DC motor driving the leadscrew of the linear actuator. The test results shown here were done at a relatively slow speed of approximately 8 mm/min, but other speeds are being tested.

Results

Initial tests with 4 and 6 inch wafers using the prototype tool show good uniformity with thickness ranges from 5-35 μ m and a smooth surface. The samples also show improvement in usable area per wafer and reductions in roughness compared to earlier tests with the old blade-style tool. Test results are repeatable, but more testing and measurements need to be performed to develop a relationship between peeling angle, force, and crack depth.



FIGURE 3. Exfoliated film sample. Silicon side up with nickel backing.

Figure 3 shows an example of film exfoliated using the prototype tool. The ceiling tiles are clearly visible reflected on the surface; there is no patterning on this sample.

METROLOGY

Critical to improving the exfoliation processes is being able to measure and quantify the produced films. Fully characterizing the process requires thickness profile measurements for both the exfoliated film and the electro-deposited nickel across as much of the wafer as possible. A curvature profile is also necessary to define the stress state. These measurements presented some significant challenges due to the necessary vertical resolution of a few microns and horizontal range spanning the entire wafer. The unsupported silicon film is also very brittle and can only be handled with a backing layer which eliminated all available direct measurement methods. The solution was to use a combination of dual KEYENCE LK-H207K laser displacement sensors (shown in Figure 4) for point thickness measurements and an Olympus OLS-4100 confocal microscope for long profile scans to

build a complete metrology map. Data processing and synthesis was performed in MATLAB.



FIGURE 4. KEYENCE differential laser displacement thickness measurement system.

Confocal line scans were taken between each stage of the process in a radial pattern and then leveled and subtracted from each other to find the film profiles. Point thickness measurements were also taken between stages in a defined grid

pattern and combined with the lines scans to create a thickness profile. After the wafer has been through the thermal annealing process another set of lines scans are taken to define the curvature of wafer. The film thickness data, together with the post-anneal curvature profile can be used to estimate the stress state in the nickel using a modified Stoney's equation for (100) silicon wafers [5]. The results are shown in Figure 5.

The correlations between the nickel thickness and nickel stress and the resulting silicon film thickness can be inferred from the plots and the broad picture provided by the data will help build the relationship between the film thicknesses and stress state. This data helps inform and validate the FEA model being developed which is presented below.

MODELING

To better understand the ideal load that the tool would apply, a 2D FEA fracture mechanics model was created using ANSYS Mechanical's Fracture Tools. Previous work in the field of thin-film interfacial fracture mechanics indicates that a stable crack path in the substrate, parallel to the

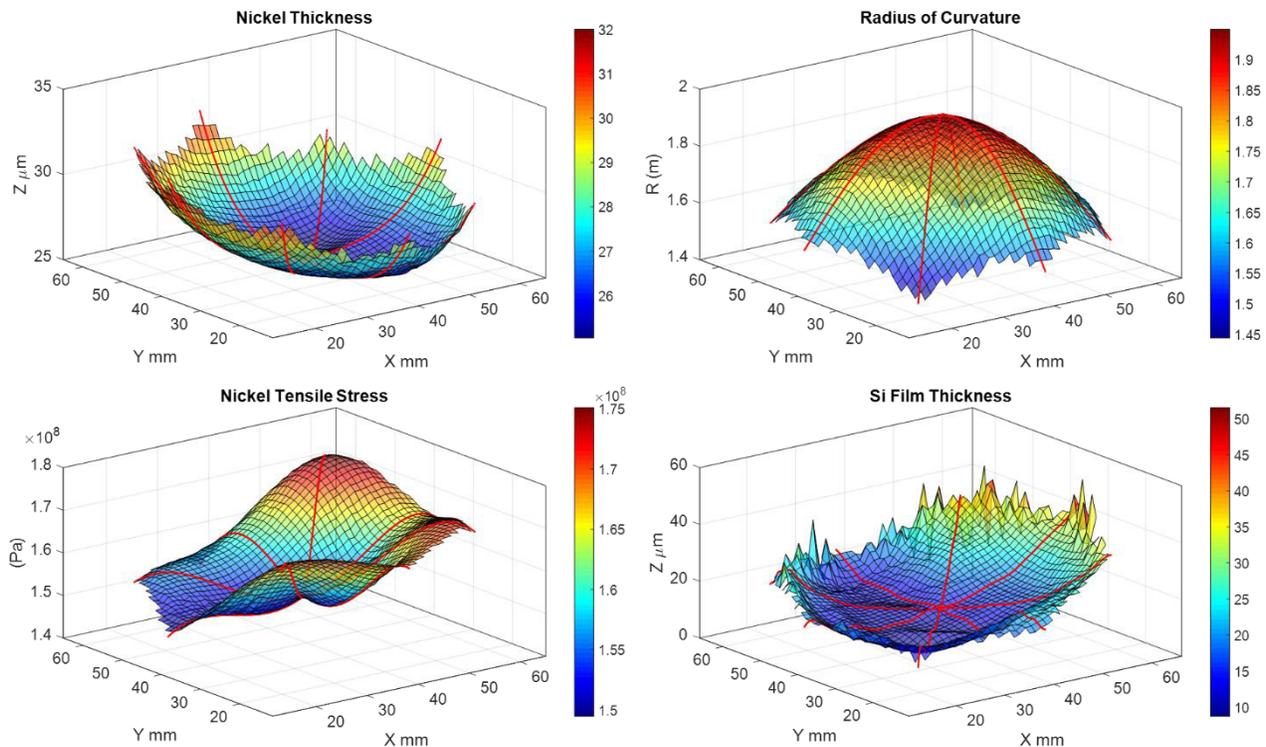


FIGURE 5. Metrology Surface Mapping. Red lines represent actual data, surface grid is a basic interpolation to aid visualization.

surface occurs when $K_{II}=0$ and that there is a characteristic crack depth for a given elastic system [6]. In this case the system is defined by the material properties, the film thickness, and the film stress for which the model can be run iteratively to solve for the characteristic crack depth. The purpose of the FEA model is to understand how to manipulate the characteristic crack depth when an external load is applied. Initial results from this FEA model and the analytical solutions from [4] indicate that changing the angle of the applied load will skew the mode mix ratio and therefore the characteristic crack depth. The final goal of the model is to form a complete design space that defines the produced film thickness for any given system and external load. The parameters could then be input into the new exfoliation tool which is presented below.

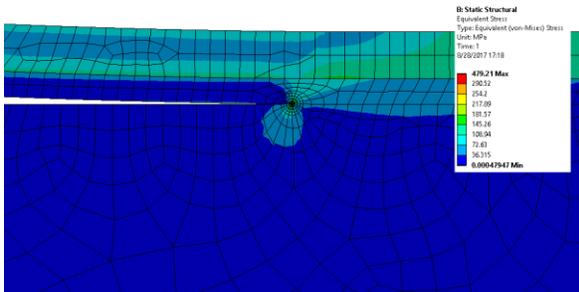


FIGURE 4. 2D FEA fracture model stress map

Figure 6 shows an example solution of the model with a layer of internally loaded nickel on top of the silicon substrate with a crack beneath the surface. The surface map shown is the equivalent stress of a typical crack system at its characteristic depth. K_I and K_{II} are calculated from the stress field.

Future Work

In the future, we will complete a design space exploration of the elastic system using the FEA model described above and validate test points using the current prototype. Information from those tests will be used to design and build an optimal tool with precision control over the external loads applied during exfoliation.

CONCLUSION

We have successfully demonstrated an exfoliation process to produce micron-scale single crystal silicon films over a wafer scale area. The construction of this tool and model provides

the basis for scalable large area monocrystalline thin film devices.

ACKNOWLEDGEMENTS

The authors acknowledge and thank Miaomiao Yang for her experience, effort, insight, and support in accomplishing this work.

This work was supported in part by the National Science Foundation Nanosystems Engineering Research Center on Nanomanufacturing Systems for Mobile Computing and Mobile Energy Technologies (NASCENT), NSF EEC Grant No.1160494 and in part by the National Science Foundation Scalable Nanomanufacturing Program, NSF Contract No. ECCS-1120823. Any opinions, findings and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the National Science Foundation. The author acknowledges the use of the NNCI facility at the Microelectronics Research Center, JJ Pickle Research Campus, UT-Austin, 10100 Burnet Rd, Austin, TX 78758.

REFERENCES

- [1] Niepelt R, Hensen J, Knorr A, Stekenreiter V, Kajari-Schöder S, Brendel R. High-quality exfoliated crystalline silicon foils for solar cell applications. *SiliconPV, Energy Procedia*. 55 (2014) 570-577.
- [2] Pang C, Lee C, Suh, K. Recent advances in flexible sensors for wearable and implantable devices. *Journal of Applied Polymer Science*. 2013; 10.1102: 1429-1441.
- [3] Rao R, Mathew L, Saha S, Smith S, Sarkar D, Garcia R, et al. A Novel Low Cost 25 μm Thin Film Exfoliated Monocrystalline Si Solar Cell Technology. *IEEE*. 2001; 978-1-4244-9965-6/11.
- [4] Bedell S, Shahrjerdi D, Fogel K, Lauro P, Bayram C, Hekmatshoar B, et al. Advanced flexible electronics: challenges and opportunities. *Proc. of SPIE*. Vol. 9083 90831G-1.
- [5] Janssen G, Abdalla M, van Keulen F. Celebrating the 100th anniversary of the Stoney equation for film stress. *Thin Solid Films*. 2009; 517 1858-1867
- [6] Drory M, Thouless M, Evans A. On the Decohesion of Residually Stressed Thin Films. *Acta metall*. 1988; Vol. 36, No.8, pp. 2019-2028